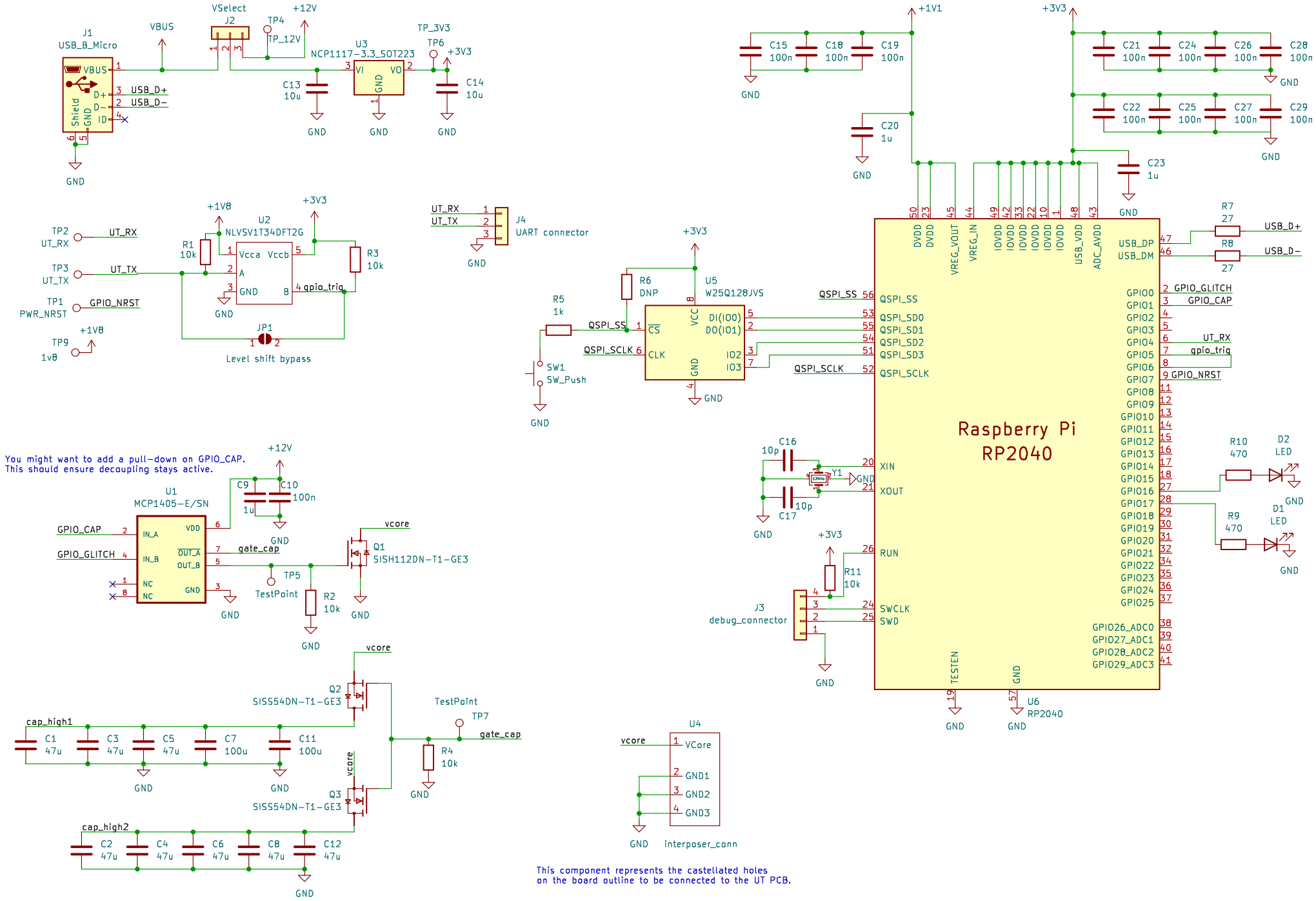
J1
USB_B_Micro
VBUS
USB_D+
USB_D−
Shield
GND
VSelect
J2
TP4
TP_12V
+12V
U3
NCP1117−3.3_SOT223
VI
VO
GND
TP_3V3
TP6
+3V3
C13
10u
C14
10u
TP2
UT_RX
TP3
UT_TX
TP1
PWR_NRST
GPIO_NRST
TP9
1v8
+1V8
U2
NLVSV1T34DFT2G
Vcca
Vccb
A
B
gpio_trig
R1
10k
R3
10k
JP1
Level shift bypass
UT_RX
UT_TX
J4
UART connector
+1V1
C15
100n
C18
100n
C19
100n
C20
1u
C21
100n
C24
100n
C26
100n
C28
100n
C22
100n
C25
100n
C27
100n
C29
100n
C23
1u
R7
27
R8
27
USB_D+
USB_D−
R5
1k
SW1
SW_Push
R6
DNP
U5
W25Q128JVS
CS
CLK
DI(IO0)
DO(IO1)
IO2
IO3
VCC
QSPI_SS
QSPI_SCLK
QSPI_SD0
QSPI_SD1
QSPI_SD2
QSPI_SD3
Raspberry Pi
RP2040
DVDD
VREG_VOUT
VREG_IN
IOVDD
USB_VDD
ADC_AVDD
USB_DP
USB_DM
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
GPIO16
GPIO17
GPIO18
GPIO19
GPIO20
GPIO21
GPIO22
GPIO23
GPIO24
GPIO25
GPIO26_ADC0
GPIO27_ADC1
GPIO28_ADC2
GPIO29_ADC3
GPIO_GLITCH
GPIO_CAP
UT_RX
gpio_trig
GPIO_NRST
C16
10p
C17
10p
Y1
12MHz
XIN
XOUT
RUN
SWCLK
SWD
TESTEN
R10
470
R9
470
D2
LED
D1
LED
R11
10k
J3
debug_connector
U6
RP2040
You might want to add a pull−down on GPIO_CAP.
This should ensure decoupling stays active.
U1
MCP1405−E/SN
IN_A
IN_B
OUT_A
OUT_B
VDD
NC
C9
1u
C10
100n
GPIO_CAP
GPIO_GLITCH
gate_cap
Q1
SISH112DN−T1−GE3
vcore
TP5
TestPoint
R2
10k
Q2
SISS54DN−T1−GE3
Q3
SISS54DN−T1−GE3
TP7
R4
10k
cap_high1
cap_high2
C1
47u
C3
47u
C5
47u
C7
100u
C11
100u
C2
47u
C4
47u
C6
47u
C8
47u
C12
47u
U4
VCore
GND1
GND2
GND3
interposer_conn
This component represents the castellated holes
on the board outline to be connected to the UT PCB.